LOW VOLTAGE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

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ABSTRACT

Operational amplifier is one of the essential component of signal processing task ranging from simple amplification of weak signal to complex audio or video processing applications in mixed signal domain. In this paper the detailed analysis of The Three Stage Operational Trans-conductance Amplifier (OTA) using active single Miller capacitor along with Inner half feed-forward technique for driving high load capacitor and comprehensive performance analysis between the active capacitive feedback compensation technique and the three stage operational trans-conductance amplifier is made. The proposed technique is implemented to work on power supply of 1.8 V while attaining amplification of more than 280 dB with increased slew rate.

KEYWORDS – Slew Rate, non-dominant complex poles, zeros

1. Introduction

Multistage amplifier has relentlessly drawn remarkable research consideration in designing. Moreover, efforts in enhancing global performance with ever growing applications demands high-gain, wide-bandwidth and fast-settling amplifiers with heavy-load and low-power conditions. The CMOS operational transconductance amplifier are one of the most versatile and imperative block in analog circuit design and mixed-signal systems. Operational Transconductance Amplifiers (OTAs) particularly provides high-precision buffering/amplifying operation, owing to their speed, area and power efficiencies under low-voltage and low-power constraints. Moreover, emerging applications such as headphone drivers, MEMS, low-dropout regulators, and active matrix display drivers, demand stringent capacitive-load capabilities higher than 1 nF increasingly urge for optimized low power frequency compensation solutions.

The proposed Technique exploits the two external feedforward stage for stability as it introduces two left half plane zeros, which further enables the non-dominant poles to shift to beyond unity gain bandwidth. Also, a novel slew rate enhancer technique is used, together with the external feedforward technique which further enables the Multistage OTA to drive high capacitive load.

The remainder of the paper is organized as follows. Firstly, the section II consists of the brief outline of DACFC Technique. Section III describes the working of the Three Stage OTA with inner half feedforward stage and the slew rate enhancer technique. The simulated results are listed in Section IV. Concluding remarks are drawn in Section V.

2. Brief Outline of DACFC

A Three-Stage Amplifier with Dual Active Capacitor Feedback Compensation Technique

The Dual Active-Capacitive-Feedback Compensation (DACFC) scheme[2] is explored for the designing of a three stage amplifier to drive large capacitive load and to operate on low-voltages. The Three-Stage Amplifier with Dual Active Capacitor Feedback Compensation Technique is better than the three stage amplifier with nested-Miller compensation scheme[3].

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The conventional nested-Miller compensation (NMC)[3] widely used methodology to stabilize a three-stage amplifier through two compensation capacitors, the bandwidth of the three-stage NMC amplifier is reduced to one quarter of that of the single-stage amplifier. The NMC structure also consists of a right-half-plane (RHP) zero, which requires a large output transconductance to ensure stability and thus makes the amplifier unsuitable for low-power design. The Three Stage OTA with DACFC structure consists of a high gain block, feedforward block and DACFC block. DACFC blocks RHP Zero by blocking feedforward current signal and creates LHP Zero by parallel combination of R_s and C_a. Further, the feedforward Stage generates a LHP Zero. Both left half plane zeros help in compensating the negative phase shift generated by non-dominant complex poles. Thus, it enables the non-dominant complex poles to be located at higher frequencies for bandwidth extension. Also, the stability of the system is achieved and capable of driving high capacitive load.

![Figure 1: Structure of the DACFC scheme](image)

On comparison to the conventional NMC technique, under low power conditions the bandwidth of DACFC scheme is extended as non-dominant poles are shifted to high frequencies. Further, the gain-bandwidth product (GBW) is improved and the required compensation capacitance of the amplifier is reduced. Moreover, the use of the small compensation capacitance and the presence of push-pull at the second and output stages enhance the transient response of the DACFC amplifier. With the use of DAFC scheme, the chip area is reduced to 33 times as compared to the NMC amplifier and a GBW of 4 MHz and a phase margin of 70 is achieved.

### 3. Three Stage OTA with Active Single Miller Capacitor and Inner Half-Feed Forward (ASMIHF) Technique

The ASMIHF technique [4] allows a generic three-stage amplifier to be stabilized by a small feedback compensation capacitor for driving very large capacitive loads. ASMIHF network takes an advantage of two left half-plane zeros for achieving an optimized compensation strategy. Also, it allows the non-dominant complex poles to be pushed to high frequencies upon low-power constraints. Moreover, a novel Class-B slew-rate enhancement technique further improves the driving capabilities of multistage amplifiers without significantly increasing the power consumption.
Figure 2: Proposed three-stage ASMIHF amplifier with Slew Rate Enhancer

The implementation at the transistor level of the three-stage amplifier adopting ASMIHF compensation technique is shown in Figure 2. A folded-cascode OTA consisting of transistors M1–M10 realizes the input gain stage, elicits a PMOS differential pair, M1–M2, and a low-voltage cascode current mirror, M7–M10. The differential pair transistors M1–M2 determines first-stage transconductance $g_m1$. The common-source transistors M12 and M13 implement the second and third gain stages, $g_m2$, and $g_m3$. The transistors of the basic amplifier are exploited to realize all the other transconductance stages. Explicitly, the gate of M11 is connected to the source of M8 which realizes the inner half-feedback transconductance $gmf1$, thus implementing an embedded current buffer stage $gmc1$. Similarly, the gate of the load transistor of the last stage M14 is connected to the gate of M10 to realize the other feedback transconductance $gmf2$. Thus, this configuration leads to the implementation of a class AB output stage which is capable of driving the load with a current much higher than the quiescent one. Also, the transistors M13–M14 and M11–M12, implement push-pull gain stages. Hence, the feedforward transconductances $gmf1$ and $gmf2$ can be dimensioned such that $gmf1 = g_m2$ and $gmf2 = g_m3$ so as to provide class-AB operation for the second and third stage while ensuring equal drive capability of the pull-up and pull-down transistors. Regarding the compensation capacitor, $CC$ is connected between the output and the source of M5, which implements $gmc1$. The inverting gain path required by the Miller compensation is realized by M7- M10, although the second and third stages are both inverting.

B. Slew-Rate Enhancer

Slew rate (SR) is characteristically limited by both the lumped node capacitances and the maximum current available to drive such capacitances. In this circuit, the overall SR is limited by the internal SR, $I_{1/CC}$, and external SR, $I_{3/CL}$. In spite of the class AB operation, due to the presence of high load capacitor (in the order of a few nano-farads), the output stage might be a slew rate limiting one. In order to avoid this, an additional slew rate enhancer (SRE) section is adopted for three-stage amplifier. Thus, it enables three-stage amplifier to operate with a low output stage quiescent current without degrading its slewing performance.

The SRE is made up of two symmetrical sections implemented by transistors M1H–M3H and M1L–M3L, respectively. M1H works as a voltage-controlled switch which is activated only during input voltage transients to provide additional current to the load. Whereas, in standby condition the transistor M3H is made to work in triode region. The SRE works as follows: initially M1H is OFF since its VSG is almost equal to 0 V. The current in M2H increases as positive large signal $V1$ is applied at M2H and M2L. If the amplitude of the input signal is high enough, M3H turns into the saturation region and the voltage at its drain lowers. M1H is then switched ON providing an additional charging current to $CL$. The operation of lower section is symmetrical as upper section.
SRE does not cause a significant increase in the complexity of the circuit and is suitable for any multistage amplifier, irrespective of the particular stage topology and compensation network.

4. Measurement Results

The proposed OTA can be fabricated using BCD6 technology, provided by STMicroelectronics, and is implemented using 0.18-µm CMOS Cadence Analog Design Environment. The OTA in figure 2 was designed for nominal target load capacitor and DC current consumption of 10 nF and 36 µA, respectively and supplied from 1.8 V. The external biasing circuit is used to provide extrapolated dc gain higher than 270 dB without increasing the complexity of the circuit. Figure 3 shows the AC frequency response of the OTA for $C_L=10$ nF. Comparison between DACFC and Proposed OTA with and without SRE is tabulated in Table 1.

![Figure 3(a) DC Gain of the Proposed OTA](image)

![Figure 3(b) Phase Margin of the Proposed OTA](image)

Table 1: Comparison between DACFC and ASMIHF Amplifier with and without SRE

<table>
<thead>
<tr>
<th>Parameters</th>
<th>DACFC Technique</th>
<th>ASMIHF Technique with SRE</th>
<th>ASMIHF Technique without SRE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load capacitor</td>
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<td>10 (nF)</td>
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<td>DC Gain(dB)</td>
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<td>0.18-µm CMOS</td>
<td>0.18-µm CMOS</td>
</tr>
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</table>
5. Conclusion

In this paper, comprehensive performance analysis for operational trans-conductance amplifier is presented. The synthesis result confirms that the proposed OTA methodology is suitable for low power and high amplification applications. The implementation results also show that the proposed OTA has superior performance (reduction in the power consumption, increment in gain and slew rate) compared to conventional design.

References

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